Domain Specific Processors Systems Architectures Modeling And Simulation Signal Processing And Communications

This book constitutes the refereed proceedings of the 5th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2005, held in Samos, Greece in July 2005. The 49 revised full papers presented were thoroughly reviewed and selected from 114 submissions. The papers are organized in topical sections on reconfigurable system design and implementations, processor architectures, design and simulation, architectures and implementations, system level design, and modeling and simulation.

It is essential that differently oriented specialists and students involved in image processing have a firm grasp of the necessary concepts and principles. A single-source reference that can provide this foundation, as well as a thorough explanation of the techniques involved, particularly those found in medical image processing, would be an

New design architectures in computer systems have surpassed industry expectations. Limits, which were once thought of as fundamental, have now been broken. Digital Systems and Applications details these innovations in systems design as well as cutting-edge applications that are emerging to take advantage of the fields increasingly sophisticated capabilities. This book features new chapters on parallelizing iterative heuristics, stream and wireless processors, and lightweight embedded systems. This fundamental text— Provides a clear focus on computer systems, architecture, and applications Takes a top-level view of system organization before moving on to architectural and organizational concepts such as superscalar and vector processor, VLIW architecture, as well as new trends in multithreading and multiprocessing. includes an entire section dedicated to embedded systems and their applications Discusses topics such as digital signal processing applications, circuit implementation aspects, parallel I/O algorithms, and operating systems Concludes with a look at new and future directions in computing Features articles that describe diverse aspects of computer usage and potentials for use Details implementation and performance-enhancing techniques such as branch prediction, register renaming, and virtual memory Includes a section on new directions in computing and their penetration into many new fields and aspects of our daily lives

In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should

also be used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications.

Domain-Specific ProcessorsSystems, Architectures, Modeling, and SimulationCRC Press

Increasing complexity of modern embedded systems demands system designers to ramp up their design productivity without compromising performance goals. This is promoted by modern Electronic System Level (ESL) techniques. Language-driven Exploration and Implementation of Partially Re-configurable ASIPs addresses an important segment of the ESL area by modeling partially re-configurable processors via high-level Architecture Description Language (ADL). This approach also hints an imminent evolution in the area of re-configurable system design.

This book constitutes the refereed proceedings of the 6th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2006, held in Samos, Greece on July 2006. The 47 revised full papers presented together with 2 keynote talks were thoroughly reviewed and selected from 130 submissions. The papers are organized in topical sections on system design and modeling, wireless sensor networks, processor design, dependable computing, architectures and implementations, and embedded sensor systems.

As the number of processor cores and IP blocks integrated on a single chip is steadily growing, a systematic approach to design the communication infrastructure becomes necessary. Different variants of packed switched on-chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real-time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system-on-chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

The rapid growth of the Internet has fueled the demand for enhanced watermarking and data hiding technologies and has stimulated research into new ways to implement watermarking systems in the real world. This book presents the fundamental principles of watermarking system design and discusses state-of-the-art technologies in information concealment and recovery. It highlights the requirements and challenges of applications in security, image/video indexing, hidden communications, image captioning, and transmission error recovery and concealment. It explains the foundations of digital watermarking technologies, and offers an understanding of new approaches and applications, and lays the groundwork for future developments in the field.

This book constitutes the refereed proceedings of the 20th International Conference on Architecture of Computing Systems, ARCS 2007, held in Zurich, Switzerland in March 2007. Coverage details a broad range of research topics related to basic technology, architecture, and application of computing systems with a strong focus on system aspects of pervasive computing and self organization techniques in both organic and autonomic computing.

The book provides a comprehensive description and implementation methodology for the Philips/NXP Aethereal/aelite Network-on-Chip (NoC). The presentation offers a systems perspective, starting from the system requirements and deriving and describing the resulting hardware architectures, embedded software, and accompanying design flow. Readers get an in depth view of the interconnect requirements, not centered only on performance and scalability, but also the multi-faceted, application-driven requirements, in particular composability and predictability. The book shows how these qualitative requirements are implemented in a state-of-the-art on-chip interconnect, and presents the realistic, quantitative costs.

Three approaches can be applied to determine the performance of parallel and distributed computer systems: measurement, simulation, and mathematical methods. This book introduces various network architectures for parallel and distributed systems as well as for systems-on-chips, and presents a strategy for developing a generator for automatic model derivation. It will appeal to researchers and students in network architecture design and performance analysis.

The popularity of magnetic resonance (MR) imaging in medicine is no mystery: it is non-invasive, it produces high quality structural and functional image data, and it is very versatile and flexible. Research into MR technology is advancing at a blistering pace, and modern engineers must keep up with the latest developments. This is only possible with a firm grounding in the basic principles of MR, and Advanced Image Processing in Magnetic Resonance Imaging solidly integrates this foundational knowledge with the latest advances in the field. Beginning with the basics of signal and image generation and reconstruction, the book covers in detail the signal processing techniques and algorithms, filtering techniques for MR images, quantitative analysis including image registration and integration of EEG and MEG techniques with MR, and MR spectroscopy techniques. The final section of the book explores functional MRI (fMRI) in detail, discussing fundamentals and advanced exploratory data analysis, Bayesian inference, and nonlinear analysis. Many of the results presented in the book are derived from the contributors' own work, imparting highly practical experience through experimental and numerical methods. Contributed by international experts at the forefront of the field, Advanced Image Processing in Magnetic Resonance Imaging is an indispensable guide for anyone interested in further advancing the technology and capabilities of MR imaging.

On behalf of the program committee, we were pleased to present this year's program for ACSAC: Asia-Paci?c Computer Systems Architecture Conference. Now in its ninth year, ACSAC continues to provide an excellent forum for researchers, educators and practitioners to come to the Asia-Paci?c region to exchange ideas on the latest developments in computer systems architecture. This year, the paper submission and review processes were semiautomated using the free version of CyberChair. We received 152 submissions, the largest number ever.Eachpaperwasassignedatleastthree,mostlyfour,andinafewcaseseven ?ve committee members for review. All of the papers were reviewed in a t- monthperiod,duringwhichtheprogramchairsregularlymonitoredtheprogress of the review process. When reviewers claimed inadequate expertise, additional reviewers were solicited. In the end, we received a total of 594 reviews (3.9 per paper) from committee members as well as 248 coreviewers whose names are acknowledged in the proceedings. We would like to thank all of them for their time and e?ort in providing us with such timely and high-quality reviews, some of them on extremely short notice.

"This book presents current research on all aspects of domain-specific language for scholars and practitioners in the software engineering fields, providing new results and answers to open problems in DSL research"--

Ranging from low-level application and architecture optimizations to high-level modeling and exploration concerns, this authoritative reference compiles essential research on various levels of abstraction appearing in embedded systems and software design. It promotes platform-based design for improved system implementation and modeling and enhanced performance and cost analyses. Domain-Specific Processors relies upon notions of concurrency and parallelism to satisfy performance and cost constraints resulting from increasingly complex applications and architectures and addresses concepts in specification, simulation, and verification in embedded systems and software design.

Satisfiability (SAT) related topics have attracted researchers from various disciplines: logic, applied areas such as planning, scheduling, operations research and combinatorial optimization, but also theoretical issues on the theme of complexity and much more, they all are connected through SAT. My personal interest in SAT stems from actual solving: The increase in power of modern SAT solvers over the past 15 years has been phenomenal. It has become the key enabling technology in automated verification of both computer hardware and software. Bounded Model Checking (BMC) of computer hardware is now probably the most widely used model checking technique. The counterexamples that it finds are just satisfying instances of a Boolean formula obtained by unwinding to some fixed depth a sequential circuit and its specification in linear temporal logic. Extending model checking to software verification is a much more difficult problem on the frontier of current research. One promising approach for languages like C with finite word-length integers is to use the same idea as in BMC but with a decision procedure for the theory of bit-vectors instead of SAT. All decision

procedures for bit-vectors that I am familiar with ultimately make use of a fast SAT solver to handle complex formulas. Decision procedures for more complicated theories, like linear real and integer arithmetic, are also used in program verification. Most of them use powerful SAT solvers in an essential way. Clearly, efficient SAT solving is a key technology for 21st century computer science. I expect this collection of papers on all theoretical and practical aspects of SAT solving will be extremely useful to both students and researchers and will lead to many further advances in the field.' Edmund Clarke (FORE Systems University Professor of Computer Science and Professor of Electrical and Computer Engineering at Carnegie Mellon University)

Modern embedded systems come with contradictory design constraints. On one hand, these systems often target mass production and battery-based devices, and therefore should be cheap and power efficient. On the other hand, they still need to show high (sometimes real-time) performance, and often support multiple applications and standards which requires high programmability. This wide spectrum of design requirements leads to complex heterogeneous System-on-Chip (SoC) architectures -- consisting of several types of processors from fully programmable microprocessors to configurable processing cores and customized hardware components, integrated on a single chip. This study targets such multiprocessor embedded systems and strives to develop algorithms, methods, and tools to deal with a number of fundamental problems which are encountered by the system designers during the early design stages.

The hand is quicker than the eye. In many cases, so is digital video. Maintaining image quality in bandwidth- and memory-restricted environments is quickly becoming a reality as thriving research delves ever deeper into perceptual coding techniques, which discard superfluous data that humans cannot process or detect. Surveying the topic from a Human Visual System (HVS)-based approach, Digital Video Image Quality and Perceptual Coding outlines the principles, metrics, and standards associated with perceptual coding, as well as the latest techniques and applications. This book is divided broadly into three parts. First, it introduces the fundamental theory, concepts, principles, and techniques underlying the field, such as the basics of compression, HVS modeling, and coding artifacts associated with current well-known techniques. The next section focuses on picture quality assessment criteria; subjective and objective methods and metrics, including vision model based digital video impairment metrics; testing procedures; and international standards regarding image quality. Finally, practical applications come into focus, including digital image and video coder designs based on the HVS as well as post-filtering, restoration, error correction, and concealment techniques. The permeation of digital images and video throughout the world cannot be understated. Nor can the importance of preserving quality while using minimal storage space, and Digital Video Image Quality and Perceptual Coding provides the tools necessary to accomplish this goal. Instructors and lecturers wishing to make use of this work as a textbook can download a presentation of 786 slides in PDF format organized to augment the text. accompany our book (H.R. Wu and K.R. Rao, Digital Video Image Quality and Perceptual Coding, CRC Press (ISBN: 0-8247-2777-0), Nov. 2005) for lecturers or instructor to use for their classes if they use the book.

This book constitutes the refereed proceedings of the 4th International Workshop on Systems, Architectures, Modeling, and Simulation,

SAMOS 2004, held in Samos, Greece on July 2004. Besides the SAMOS 2004 proceedings, the book also presents 19 revised papers from the predecessor workshop SAMOS 2003. The 55 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in topical sections on reconfigurable computing, architectures and implementation, and systems modeling and simulation.

Scenario -- Groundwork -- Structure -- Meaning -- Modeling processes -- Communication -- Navigation and discovery -- Presentation formats -- Infrastructure -- Solutions.

This book constitutes the proceedings of the 27th International Conference on Architecture of Computing Systems, ARCS 2014, held in Lübeck, Germany, in February 2014. The 20 papers presented in this volume were carefully reviewed and selected from 44 submissions. They are organized in topical sections named: parallelization: applications and methods; self-organization and trust; system design; system design and sensor systems; and virtualization: I/O, memory, cloud; dependability: safety, security, and reliability aspects.

Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices addresses a subject that is becoming more important over the years. On the one hand the arrival of home networks is imminent, and on the other hand we notice that chips integrate more and more functionality. The home network interconnects the Consumer Electronic (CE) devices in the home, and the individual CE-devices incorporate the chips to realize a ubiquitous streaming of video streams over this network. This book provides a comprehensive overview of the challenges that face us. The book shows that there are many similarities between traditional networking and networks in the chip. However, there are some different operational conditions that lead to original solutions. Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices focuses on the robustness aspects of the chosen technologies in the area of video streaming. Management of resources such as memory, bandwidth, CPU cycles, bus–cycles is an aspect that is prominent in many of the sections.

This reference presents a more efficient, flexible, and manageable approach to unitary transform calculation and examines novel concepts in the design, classification, and management of fast algorithms for different transforms in one-, two-, and multidimensional cases. Illustrating methods to construct new unitary transforms for best algorithm selection and development in real-world applications, the book contains a wide range of examples to compare the efficacy of different algorithms in a variety of one-, two-, and three-dimensional cases. Multidimensional Discrete Unitary Transforms builds progressively from simple representative cases to higher levels of generalization.

This book constitutes the refereed proceedings of the 5th IFIP TC 10 International Embedded Systems Symposium, IESS 2015, held in Foz do Iguaçu, Brazil, in November 2015. The 18 full revised papers presented were carefully reviewed and selected from 25 submissions. The papers present a broad discussion on the design, analysis and verification of embedded and cyber-physical systems including design methodologies, verification, performance analysis, and real-time systems design. They are organized in the following topical sections: cyber-physical systems, system-level design; multi/many-core system design; memory system design; and embedded HW/SW design and applications.

After nearly six years as the field's leading reference, the second edition of this award-winning handbook reemerges with completely updated content and a brand new format. The Computer Engineering Handbook, Second Edition is now offered as a set of two carefully focused books that together encompass all aspects of the field. In addition to complete updates throughout the book to reflect the latest issues in low-power design, embedded processors, and new standards, this edition includes a new section on computer memory and storage as well as several new chapters on such topics as semiconductor memory circuits, stream and wireless processors, and nonvolatile memory

technologies and applications.

Ranging from low-level application and architecture optimizations to high-level modeling and exploration concerns, this authoritative reference compiles essential research on various levels of abstraction appearing in embedded systems and software design. It promotes platform-based design for improved system implementation and modeling and enhanced

The SAMOS workshop is an international gathering of highly quali?ed researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the sci-ti?c arena. Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I–IV (2001–2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), T- wan (1), Turkey (2), UK (2), and USA (5). We are grateful to all of the authors who submitted papers to the workshop.

Showcasing the most influential developments, experiments, and architectures impacting the digital, surveillance, automotive, industrial, and medical sciences, this text/reference tracks the evolution and advancement of CVIP technologies - examining methods and algorithms for image analysis, optimization, segmentation, and restoration.

Today more than 90% of all programmable processors are employed in embedded systems. The LISA processor design platform presented in this book addresses recent design challenges and results in highly satisfactory solutions, covering all major high-level phases of embedded processor design.

This is volume 75 of Advances in Computers. This series, which began publication in 1960, is the oldest continuously published anthology that chronicles the ever- changing information technology field. In these volumes we publish from 5 to 7 chapters, three times per year, that cover the latest changes to the design, development, use and implications of computer technology on society today. In this present volume we present five chapters describing new technology affecting users of such machines. In this volume we continue a theme presented last year in volume 72 – High Performance Computing. In volume 72 we described several research projects being conducted in the United States on

the development of a new generation of high performance supercomputers.

Integrated System-Level Modeling of Network-on-Chip Enabled Multi-Processor Platforms first gives a comprehensive update on recent developments in the area of SoC platforms and ESL design methodologies. The main contribution is the rigorous definition of a framework for modeling at the timing approximate level of abstraction. Subsequently this book presents a set of tools for the creation and exploration of timing approximate SoC platform models.

Modern consumers carry many electronic devices, like a mobile phone, digital camera, GPS, PDA and an MP3 player. The functionality of each of these devices has gone through an important evolution over recent years, with a steep increase in both the number of features as in the quality of the services that they provide. However, providing the required compute power to support (an uncompromised combination of) all this functionality is highly non-trivial. Designing processors that meet the demanding requirements of future mobile devices requires the optimization of the embedded system in general and of the embedded processors in particular, as they should strike the correct balance between flexibility, energy efficiency and performance. In general, a designer will try to minimize the energy consumption (as far as needed) for a given performance, with a sufficient flexibility. However, achieving this goal is already complex when looking at the processor in isolation, but, in reality, the processor is a single component in a more complex system. In order to design such complex system successfully, critical decisions during the design of each individual component should take into account effect on the other parts, with a clear goal to move to a global Pareto optimum in the complete multi-dimensional exploration space. In the complex, global design of battery-operated embedded systems, the focus of Ultra-Low Energy Domain-Specific Instruction-Set Processors is on the energy-aware architecture exploration of domain-specific instruction-set processors and the co-optimization of the datapath architecture, foreground memory, and instruction memory organisation with a link to the required mapping techniques or compiler steps at the early stages of the design. By performing an extensive energy breakdown experiment for a complete embedded platform, both energy and performance bottlenecks have been identified, together with the important relations between the different components. Based on this knowledge, architecture extensions are proposed for all the bottlenecks.

The past few years have seen significant change in the landscape of high-end network processing. In response to the formidable challenges facing this emerging field, the editors of this series set out to survey the latest research and practices in the design, programming, and use of network processors. Through chapters on hardware, software, performance and modeling, Network Processor Design illustrates the potential for new NP applications, helping to lay a theoretical foundation for the architecture, evaluation, and programming of networking processors. Like Volume 2 of the series, Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing

other critical factors such as ease of programming, application developments, power, and performance prediction. In addition, Volume 3 emphasizes forward-looking, leading-edge research in the areas of architecture, tools and techniques, and applications such as high-speed intrusion detection and prevention system design, and the implementation of new interconnect standards. Investigates current applications of network processor technology at Intel; Infineon Technologies; and NetModule Presents current research in network processor design in three distinct areas: Architecture at Washington University, St. Louis; Oregon Health and Science University; University of Georgia; and North Carolina State University. Tools and Techniques at University of Texas, Austin; Academy of Sciences, China; University of Paderborn, Germany; and University of Massachusetts, Amherst. Applications at University of California, Berkeley; Universidad Complutense de Madrid, Spain; ETH Zurich, Switzerland; Georgia Institute of Technology; Vrije Universiteit, the Netherlands; and Universiteit Leiden, the Netherlands.

Broadband Last Mile: Access Technologies for Multimedia Communications provides in-depth treatments of access technologies and the applications that rely upon them or support them. It examines innovations and enhancements along multiple dimensions in access, with the overarching goal of ensuring that the last mile is not the weak link in the broadband chain. Written by experts from the academic and commercial segments of the field, the book's self-contained sections address topics related to the disciplines of communications, networking, computing, and signal processing. The core of this treatment contains contemporary reviews of broadband pipes in the classes of copper, cable, fiber, wireless, and satellite. It emphasizes the coexistence of these classes within a network, the importance of optical communications for unprecedented bandwidth, and the flexibility and mobility provided by wireless. The book also includes perspective on the increasingly important topic of network management, providing insights that are true regardless of the nature of the pipe. The text concludes with a discussion of newly emerging applications and broadband services. This book offers an all-in-one treatment of the physical pipes and network architectures that make rich and increasingly personalized applications possible. It serves as a valuable resource for researchers and practitioners working in the increasingly pervasive field of broadband.

Taking another lesson from nature, the latest advances in image processing technology seek to combine image data from several diverse types of sensors in order to obtain a more accurate view of the scene: very much the same as we rely on our five senses. Multi-Sensor Image Fusion and Its Applications is the first text dedicated to the theory and practice of the registration and fusion of image data, covering such approaches as statistical methods, color-related techniques, model-based methods, and visual information display strategies. After a review of state-of-the-art image fusion techniques, the book provides an overview of fusion algorithms and fusion performance evaluation. The following

chapters explore recent progress and practical applications of the proposed techniques to solving problems in such areas as medical diagnosis, surveillance and biometric systems, remote sensing, nondestructive evaluation, blurred image restoration, and image quality assessment. Recognized leaders from industry and academia contribute the chapters, reflecting the latest research trends and providing useful algorithms to aid implementation. Supplying a 28-page full-color insert, Multi-Sensor Image Fusion and Its Applications clearly demonstrates the benefits and possibilities of this revolutionary development. It provides a solid knowledge base for applying these cutting-edge techniques to new challenges and creating future advances.

This textbook is intended to give an introduction to and an overview of sta- of-the-art techniques in the design of complex embedded systems. The book title is SAMOS for two major reasons. First, it tries to focus on the actual distinct, yet important problem ?elds of System-Level design of embedded systems, including mapping techniques and synthesis,Architectural design,Modeling issues such as speci?cation languages, formal models, and- nallySimulation. The second reason is that the volume includes a number of papers presented at a workshop with the same name on the Island of Samos, Greece, in July 2001. In order to receive international attention, a number of reputed researchers were invited to this workshop to present their current work. Participation was by invitation only. For the volume presented here, a number of additional papers where selected based on a call for papers. All contributions were refereed. This volume presents a selection of 18 of the refereed papers, including 2 invited papers. The textbook is organized according to four topics: The ?rst isA)System- LevelDesignandSimulation.Inthissection,wepresentacollectionofpapers that give an overview of the challenging goal to design and explore alternatives of embedded system implementations at the system-level. One paper gives an overview of models and tools used in system-level design. The other papers present new models to describe applications, provide models for re?nement and design space exploration, and for tradeo? analysis between cost and ?exibility of an implementation.

This book constitutes the refereed proceedings of the 8th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2008, held in Samos, Greece, in July 2008. The 24 revised full papers presented together with a contamplative keynote and additional papers of two special workshop sessions were carefully reviewed and selected from 62 submissions. The papers are organized in topical sections on architecture, new frontiers, SoC, application specific contributions, system level design for heterogeneous systems, programming multicores, sensors and sensor networks; and systems modeling and design.

The two volumes LNCS 8805 and 8806 constitute the thoroughly refereed post-conference proceedings of 18 workshops held at the 20th International Conference on Parallel Computing, Euro-Par 2014, in Porto, Portugal, in August 2014. The

100 revised full papers presented were carefully reviewed and selected from 173 submissions. The volumes include papers from the following workshops: APCI&E (First Workshop on Applications of Parallel Computation in Industry and Engineering - BigDataCloud (Third Workshop on Big Data Management in Clouds) - DIHC (Second Workshop on Dependability and Interoperability in Heterogeneous Clouds) - FedICI (Second Workshop on Federative and Interoperable Cloud Infrastructures) - Hetero Par (12th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms) - HiBB (5th Workshop on High Performance Bioinformatics and Biomedicine) - LSDVE (Second Workshop on Large Scale Distributed Virtual Environments on Clouds and P2P) - MuCoCoS (7th International Workshop on Multi-/Many-core Computing Systems) - OMHI (Third Workshop on On-chip Memory Hierarchies and Interconnects) - PADAPS (Second Workshop on Parallel and Distributed Agent-Based Simulations) - PROPER (7th Workshop on Productivity and Performance) - Resilience (7th Workshop on Resiliency in High Performance Computing with Clusters, Clouds, and Grids) - REPPAR (First International Workshop on Reproducibility in Parallel Computing) - ROME (Second Workshop on Runtime and Operating Systems for the Many Core Era) - SPPEXA (Workshop on Software for Exascale Computing) - TASUS (First Workshop on Techniques and Applications for Sustainable Ultrascale Computing Systems) - UCHPC (7th Workshop on Un Conventional High Performance Computing) and VHPC (9th Workshop on Virtualization in High-Performance Cloud Computing.
Relying heavily on MATLAB® problems and examples, as well as simulated data, this text/reference surveys a vast array of signal and image processing tools for biomedical applications, providing a working knowledge of the technologies addressed while showcasing valuable implementation procedures, common pitfalls, and essential application concepts. The first and only textbook to supply a hands-on tutorial in biomedical signal and image processing, it offers a unique and proven approach to signal processing instruction, unlike any other competing source on the topic. The text is accompanied by a CD with support data files and software including all MATLAB examples and figures found in the text.
Network on Chip (NoC) addresses the communication requirement of different nodes on System on Chip. The bio-inspired algorithms improve the bandwidth utilization, maximize the throughput and reduce the end-to-end latency and inter-flit arrival time. This book exclusively presents in-depth information regarding bio-inspired algorithms solving real world problems focussing on fault-tolerant algorithms inspired by the biological brain and implemented on NoC. It further documents the bio-inspired algorithms in general and more specifically, in the design of NoC. It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters. Key Features: Covers bio-inspired solutions pertaining to Network-on-Chip (NoC) design solving real world examples Includes bio-inspired NoC fault-tolerant algorithms with detail coding examples Lists fault-tolerant algorithms with detailed

examples Reviews basic concepts of NoC Discusses NoC architectures developed-to-date